UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,088	02/05/2004	Mitsuru Okigawa	81784.0301	3288

7590 12/21/2005

HOGAN & HARTSON L.L.P.
Biltmore Tower
Suite 1900
500 South Grand Avenue
Los Angeles, CA 90071

EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/773,088	OKIGAWA, MITSURU	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 9* is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 10/24/05.

Claims **1-9** are pending in this application.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 5-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification, as originally filed, does not disclose that "... a first step of coating resin mixed with micro-particles on at least *one surface of a semiconductor substrate on which a semiconductor integrated circuit is formed*, and laminating a support substrate on the semiconductor substrate to hold the resin between the two substrate; and ... wherein *no connection terminals are provided between the surface of the semiconductor substrate and the support substrate* ...", as recited in independent claim 5.

Claims 6-7 are rejected since each includes the limitations of independent claim 5.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims **5-7** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim **5**, the recitations "... *a first step of coating resin mixed with micro-particles on at least* ***one surface of a semiconductor substrate on which a semiconductor integrated circuit is formed,*** *and laminating a support substrate on the semiconductor substrate to hold the resin between the two substrate; and ... wherein* ***no connection terminals are provided between the surface of the semiconductor substrate and the support substrate*** ..." is not understood of how *a semiconductor surface, on which a semiconductor integrated circuit is formed, has no connection terminals.*

Claims **6-7** are rejected since each includes the limitations of independent claim **5**.

See that the claims above have been rendered indefinite and many 112 problems. Therefore, the examiner has examined the claims as best understood by the examiner.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Connell et al. (6,791,168 hereinafter "Connell").

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-4, Connell (see specifically figure 8B) discloses a semiconductor integrated device, comprising: a semiconductor substrate (135) having a semiconductor integrated circuit formed thereon, a support substrate (42A) on which the semiconductor substrate (135) mounted, a resin (137/64A) filled between the semiconductor substrate (135) and the support substrate (42A), where in the resin contains a first resin layer (137) that is a mixture of micro-particles (Col. 9, lines 31+) and a second resin layer (64A) not containing micro-particles, and wherein no connection terminals are provided between the surface of the semiconductor substrate (135) and the support substrate (42A) (see figure 8B), and wherein a distance between the semiconductor substrate and the support substrate is larger than the maximum particle diameter of the micro particles (since the second resin layer 64A is not containing micro-particles). Connell further discloses the step of etching to reduce the thickness of the semiconductor substrate (Col. 6, lines 16+).

It should be noted that although claims 5-7 are "method claims", the method steps consist of the broad steps of "coating...., laminating...., pushing.....etc.", therefore these steps would be inherently satisfied by the apparatus of the reference as modified.

Regarding claims 1-2, Connell (see specifically figures 1A-1B) discloses a semiconductor integrated device, comprising: resin (26) mixed with micro particles on at least one surface of a semiconductor substrate (16) on which a semiconductor integrated circuit is formed, and laminating a support substrate (12) on the semiconductor substrate

to hold the resin (26) between the two substrates (12/16), wherein no connection terminals are provided between the surface of the semiconductor substrate (16) and the support substrate (12) (see figures 1A-1B), and wherein a distance between the semiconductor substrate and the support substrate is larger than the maximum particle diameter of the micro particles (Col. 8, lines 45-47). Connell further discloses the step of etching to reduce the thickness of the semiconductor substrate (Col. 6, lines 16+).

Allowable Subject Matter

1. Claims 8-9 are allowed.

2. The following is an examiner's statement of reasons for allowance:

There was no prior art found by the examiner that suggested modification or combination with the cited prior art so as to satisfy the combination of the present independent claim 8. Especially, the prior arts fail to teach or fairly suggest, among others, at least the method steps of: *hardening a first resin layer mixed with micro-particles coated on at least one surface of a semiconductor substrate on which a semiconductor integrated circuit is formed; and coating a second resin layer not containing micro-particles on the first resin layer hardened in the previous step, wherein hardening (the first resin layer mixed with micro-particles) is carried out so that the film thickness of the first resin layer after hardening is kept larger than the maximum particle diameter of the micro-particles.*

Conclusion

6. Applicant's arguments with respect to claims **1-7** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

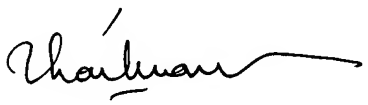
7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the underlined portions of claims 1 and 5 raise new issues that would require further consideration and/or search. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luan Thai
Primary Examiner
Art Unit 2891
December 16, 2005